Abstract of the Disclosure

A transceiving network controller that controls memory allocation of a buffer memory according to data flow and a method for controlling memory allocation and data flow. The transceiving network controller comprises a system bus, a buffer memory including a transmitting area capable of flexible memory allocation according to transmitted data flow and a receiving area capable of flexible memory allocation according to received data flow, the buffer memory for storing and outputting transmitted data in response to at least one transmitting address signal and for storing and outputting received data in response to at least one receiving address signal, a flow control unit for generating and outputting threshold control signals for increasing the memory allocation of the transmitting area when a transmission execution signal becomes active and for increasing the memory allocation of the receiving area when a reception execution signal becomes active, a transmitting controller for generating a plurality of transmitting address signals, and a receiving controller for generating a plurality of receiving address signals.

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